

Integrated Systems

Continuous-Time Pipelined Analog-to-Digital Converters – Where Filtering Meets Analog-to-Digital Conversion

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Refreshments will be served

Abstract: If someone told you that the power, noise, distortion, and area of a mixed-signal block could be reduced all at the same time, you'd probably think that this was a lie. It turns out that it is indeed possible sometimes - and this talk will present an example called the continuous-time pipeline (CTP) ADC. The CTP is an emerging technique that combines filtering with analog-to-digital conversion. Like a continuous-time delta-sigma modulator (CTDSM), a CTP has a "nice" input impedance that is easy to drive and has inherent anti-aliasing. However, unlike a CTDSM, a CTP does not require a high-speed feedback loop to be closed. As a result, it can achieve significantly higher bandwidth (like a Nyquist ADC). After discussing the operating principles behind the CTP, we describe the fundamental benefits of the CTP over a conventional signal chain that incorporates an anti-alias filter and a Nyquist-rate converter. We will then show design details and measurement results from a 100MHz 800MS/s CTP designed in a 65nm CMOS process.



Biography: Shanthi Pavan received the B.Tech. degree in electronics and communication engineering from IIT Madras, Chennai, India, in 1995, and the M.S. and D.Sc. degrees from Columbia University, New York, NY, USA, in 1997 and 1999, respectively. From 1997 to 2000, he was with Texas Instruments, Warren, NJ, USA, where he worked on high-speed analog filters and data converters. From 2000 to June 2002, he worked on microwave ICs for data communication at Bigbear Networks, Sunnyvale, CA, USA. Since July 2002, he has been with IIT Madras, where he is currently the NT Alexander Institute Chair Professor of Electrical Engineering. He is the author of *Understanding Delta-Sigma Data Converters* (second edition, with Richard Schreier and Gabor Temes), which received the Wiley-IEEE Press Professional Book Award for the year 2020. His research interests are in the areas of high-speed analog circuit design and signal processing. Dr. Pavan is a fellow of the Indian National Academy of Engineering, and the recipient of several awards, including the IEEE Circuits and Systems Society Darlington Best Paper Award in 2009. He has served as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems—I: Regular Papers. He has been a Distinguished Lecturer

of the Solid-State Circuits and Circuits-and-Systems Societies. He currently serves as the Vice-President of Publications of the IEEE Solid-State Circuits Society, on the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC), and on the editorial board of the IEEE Journal of Solid-State Circuits. He is an IEEE Fellow.

Hosted by Prof. Mike Chen, Prof. Hossein Hashemi, and Prof. Constantine Sideris